Electronic Version
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Claims

[c1] A method of fabricating a FinFET semiconductor structure, comprising steps of:
forming a fin for a FinFET on a substrate, the fin having first and second sides;
introducing a first impurity on the first side of the fin; and
forming a dielectric layer on the first and second sides, wherein the dielectric layer is thicker on one of the first and second sides than the other of the first and second sides, and the introduced impurity affects dielectric layer thickness.

[c2] The method according to Claim 1, wherein the first impurity is a substance that retards dielectric layer formation.

[c3] The method according to Claim 2, wherein the first impurity includes one of nitrogen, nitrogen ions or nitrogen containing compounds.

[c4] The method according to Claim 1, wherein the first impurity is a substance that enhances dielectric layer formation.

[c5] The method according to Claim 4, wherein the first impurity includes one of silicon, argon, cesium, oxygen or germanium, or ions or compounds thereof.

[c6] The method according to Claim 1, wherein the step of introducing a first impurity is comprised of a step of directional implantation.

[c7] The method according to Claim 6, wherein the step of directional implantation includes tilting the structure to a predetermined angle of incidence with the impurity being implanted.

[c8] The method according to Claim 1, wherein the substrate is comprised of a buried oxide layer.

[c9] The method according to Claim 1, further including a step of introducing a second impurity on the second side of the fin.

[c10] The method according to Claim 9, wherein the first impurity is a substance that retards dielectric layer formation and the second impurity is a substance that enhances dielectric formation.

[c11] The method according to Claim 10, wherein:
the first impurity includes one of nitrogen, nitrogen ions or nitrogen containing compounds; and

the second impurity includes one of silicon, argon, cesium, oxygen or germanium, or ions or compounds thereof.

[c12] The method according to Claim 10, wherein:
the step of introducing a first impurity is comprised of a step of directional implantation directed to the first side of the fin; and
the step of introducing a second impurity is comprised of a step of directional implantation directed to the second side of the fin.

[c13] The method according to Claim 12, wherein the steps of directional implantation include tilting the structure to a predetermined angle of incidence with the impurity being implanted.

[c14] A method of fabricating a FinFET semiconductor structure, comprising steps of:
forming a fin for a FinFET on a substrate, the fin having first and second sides;
directionally implanting a first impurity on the first side of the fin;
forming a dielectric layer on the first and second sides, the dielectric layer being thicker on one of the first and second sides than the other of the first and second sides, due to the introduced impurity affecting dielectric

layer thickness; and

forming a FinFET gate straddling the fin, the FinFET gate having front and back gate sides and a top surface.

[c15] The method according to Claim 14, further comprising a step of backgating the back gate side of the gate.

[c16] The method according to Claim 15, wherein the step of backgating the back gate side of the gate includes applying a bias to the back gate side of the gate.

[c17] The method according to Claim 14, further comprising a step of doping the gate regions on the structure.

[c18] The method according to Claim 17, wherein an n-type impurity is implanted directionally on one side of the gate and a p-type impurity is implanted directionally on the other side of the gate.

[c19] The method according to Claim 14, further comprising a step of forming source and drain regions on the structure.

[c20] The method according to Claim 19, wherein the step of forming source and drain regions on the structure further includes:

directionally implanting a source dopant into the source region; and

directionally implanting a drain dopant into the drain region.

[c21] The method according to Claim 19, further comprising a step of forming spacers abutting the FinFET gate.

[c22] The method according to Claim 21, further comprising a step of planarizing the top surface of the gate.

[c23] A FinFET semiconductor structure, comprising:
a substrate;
a fin for a FinFET on the substrate, the fin having first and second sides;
a first impurity on the first side of the fin;
a dielectric layer on the first and second sides, the dielectric layer being thicker on one of the first and second sides than the other of the first and second sides, the introduced impurity affecting dielectric layer thickness.

[c24] The FinFET semiconductor structure according to Claim 23, further comprising a gate straddling the fin, the gate having front and back gate sides and a top surface wherein the back gate side of the gate is backgated.

[c25] The FinFET semiconductor structure according to Claim 24, wherein a bias is applied to the back gate side of the gate.

[c26] The FinFET semiconductor structure according to Claim 25, further comprising a doping the gate regions on the structure.

[c27] The FinFET semiconductor structure according to Claim 25, wherein an n-type impurity is implanted directionally on one side of the gate and a p-type impurity is implanted directionally on the other side of the gate.

[c28] The FinFET semiconductor structure according to Claim 23, further comprising source and drain regions on the structure.

[c29] The FinFET semiconductor structure according to Claim 23, further comprising
directionally implanted source dopants in the source region; and
directionally implanted drain dopants in the drain region.

[c30] The FinFET semiconductor structure according to Claim 28, further comprising spacers abutting a FinFET gate straddling the fin.

[c31] The FinFET semiconductor structure according to Claim 28, wherein the FinFET gate has a planarized top surface.